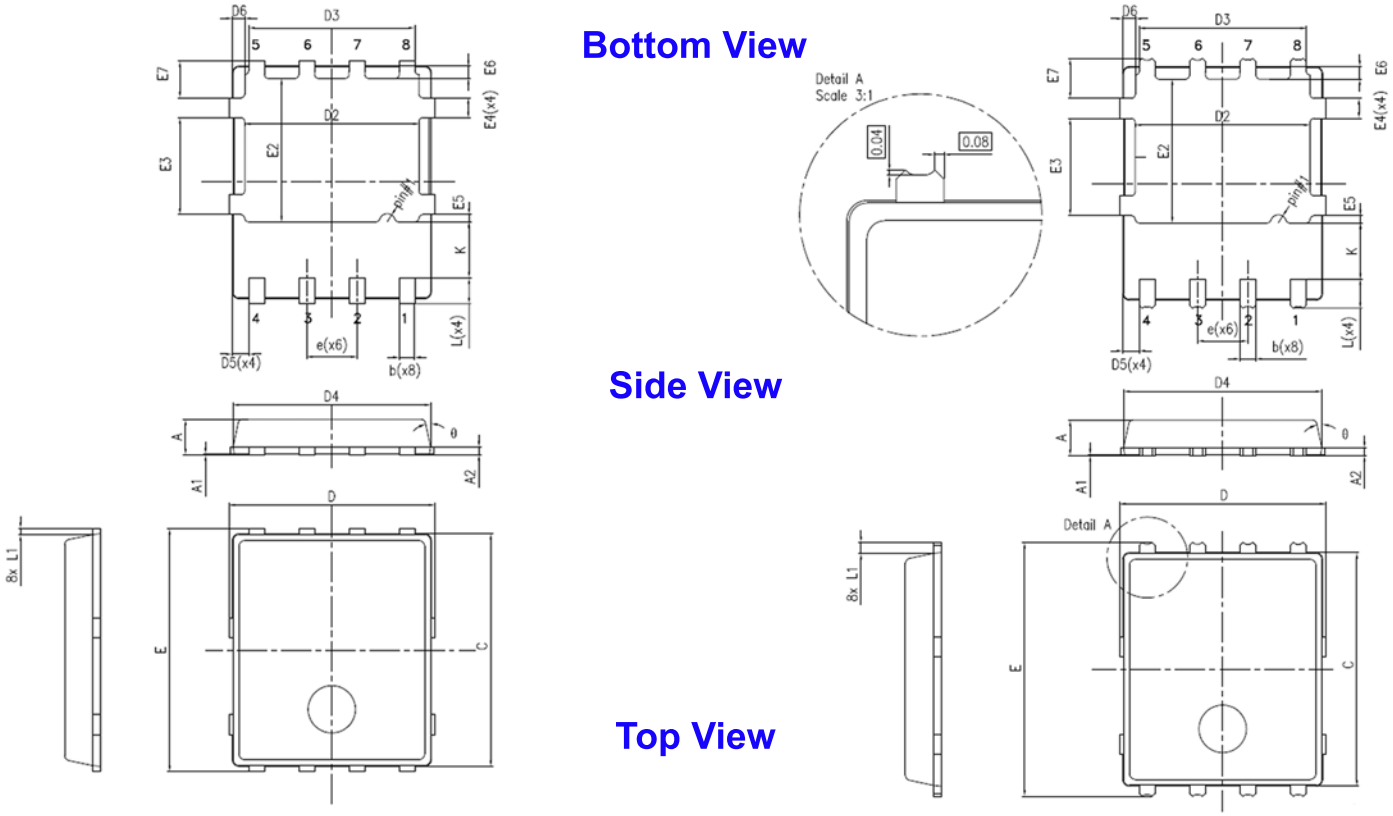
PowerFLAT™ 5x6 single island

Type R (Ribbon)

Current

Wettable Flanks



DIMENSIONS				
REF. DIM	DATA BOOK (mm)			NOTES
	NOM	MIN	MAX	
A		0.80	1.00	
A1		0.02	0.05	
A2	0.25			
b		0.30	0.50	
C	6.00	5.80	6.20	
D	5.20	5.00	5.40	
D2		4.15	4.45	
D3	4.20	4.05	4.35	
D4	5.0	4.80	5.20	
D5	0.4	0.25	0.55	
D6	0.3	0.15	0.45	
e	1.27			
E	6.15	5.95	6.35	
E2		3.50	3.70	
E3		2.35	2.55	
E4		0.40	0.60	
E5		0.08	0.28	
E6	0.325	0.2	0.450	
E7	0.90	0.75	1.05	
K		1.275	1.575	
L		0.60	0.80	
L1	0.15	0.05	0.25	
θ		0°	12°	

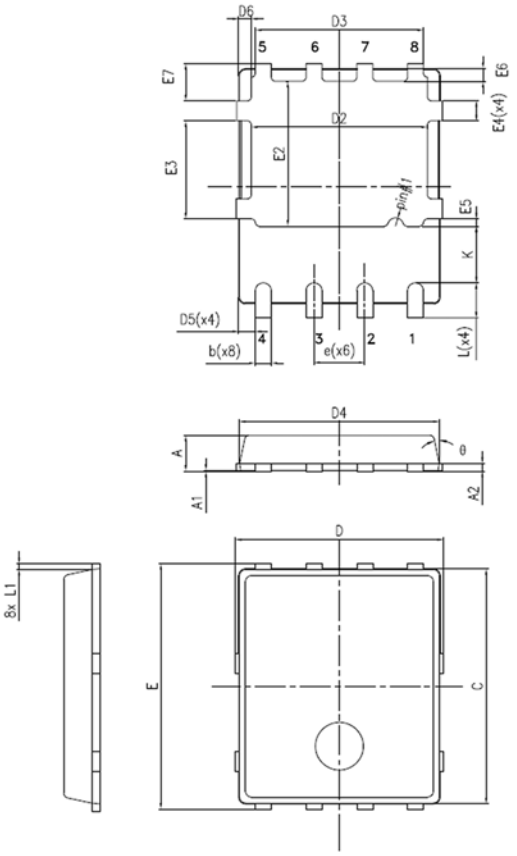
DIMENSIONS				
REF. DIM	DATA BOOK (mm)			NOTES
	NOM	MIN	MAX	
A		0.80	1.00	
A1		0.02	0.05	
A2	0.25			
b		0.30	0.50	
C	6.00	5.80	6.20	
D	5.20	5.00	5.40	
D2		4.15	4.45	
D3	4.20	4.05	4.35	
D4	5.0	4.80	5.20	
D5	0.4	0.25	0.55	
D6	0.3	0.15	0.45	
e	1.27			
E	6.40	6.20	6.60	
E2		3.50	3.70	
E3		2.35	2.55	
E4		0.40	0.60	
E5		0.08	0.28	
E6	0.325	0.175	0.450	
E7	1.00	0.85	1.15	
K		1.275	1.575	
L	0.825	0.725	0.925	
L1	0.275	0.175	0.375	
θ		0°	12°	

Remark: Comparison done with real Package, current and Wettable Flanks.
It may be different from previous drawing, present in some datasheet.

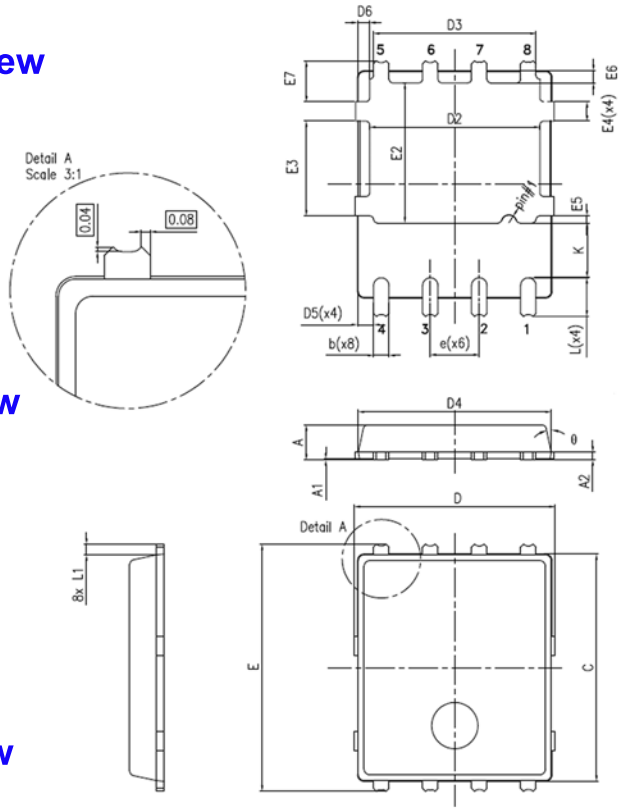
PowerFLAT™ 5x6 single island

Type C (Clip)

Current



Wettable Flanks



DIMENSIONS				
REF. DIM	DATA BOOK (mm)			NOTES
	NOM	MIN	MAX	
A		0.80	1.00	
A1		0.02	0.05	
A2	0.25			
b		0.30	0.50	
C	6.00	5.80	6.20	
D	5.20	5.00	5.40	
D2		4.15	4.45	
D3	4.20	4.05	4.35	
D4	5.0	4.80	5.20	
D5	0.4	0.25	0.55	
D6	0.3	0.15	0.45	
e	1.27			
E	6.15	5.95	6.35	
E2		3.50	3.70	
E3		2.35	2.55	
E4		0.40	0.60	
E5		0.08	0.28	
E6	0.325	0.2	0.450	
E7	0.90	0.75	1.05	
K		1.05	1.35	
L		0.715	1.015	
L1	0.15	0.05	0.25	
θ		0°	12°	

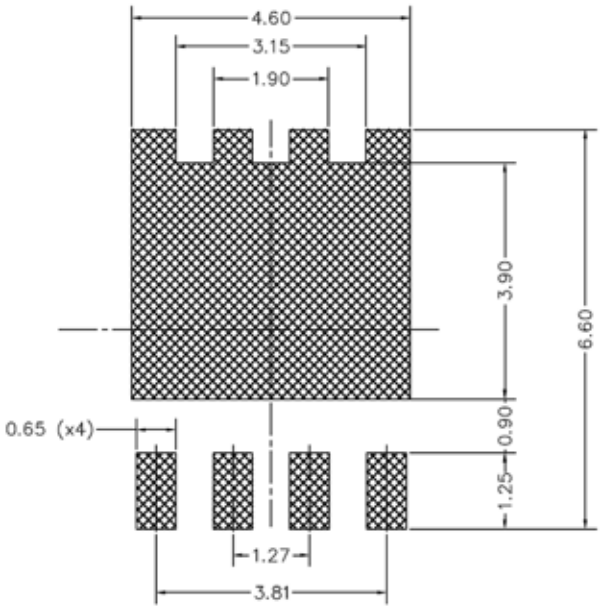
DIMENSIONS				
REF. DIM	DATA BOOK (mm)			NOTES
	NOM	MIN	MAX	
A		0.80	1.00	
A1		0.02	0.05	
A2	0.25			
b		0.30	0.50	
C	6.00	5.80	6.20	
D	5.20	5.00	5.40	
D2		4.15	4.45	
D3	4.20	4.05	4.35	
D4	5.0	4.80	5.20	
D5	0.4	0.25	0.55	
D6	0.3	0.15	0.45	
e	1.27			
E	6.40	6.20	6.60	
E2		3.50	3.70	
E3		2.35	2.55	
E4		0.40	0.60	
E5		0.08	0.28	
E6	0.325	0.2	0.450	
E7	1.00	0.85	1.15	
K		1.05	1.35	
L	1.00	0.90	1.10	
L1	0.275	0.175	0.375	
θ		0°	12°	

Remark: Comparison done with real Package, current and Wettable Flanks.
It may be different from previous drawing, present in some datasheet.

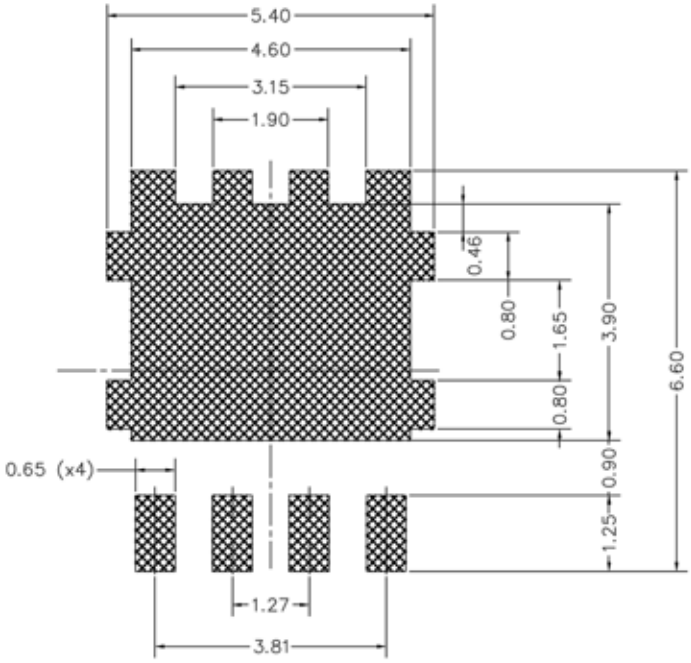
PowerFLAT™ 5x6 single island

Footprint

Current

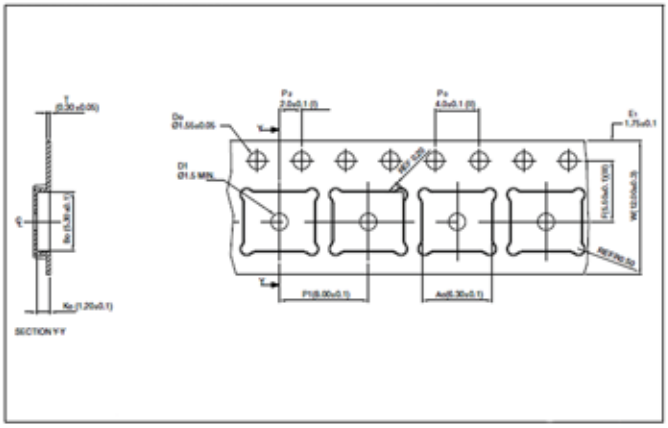


Wettable Flanks

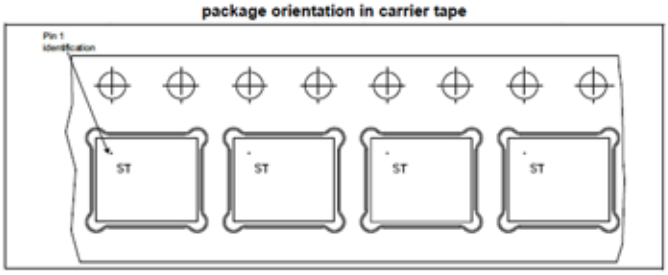


Carrier Tape

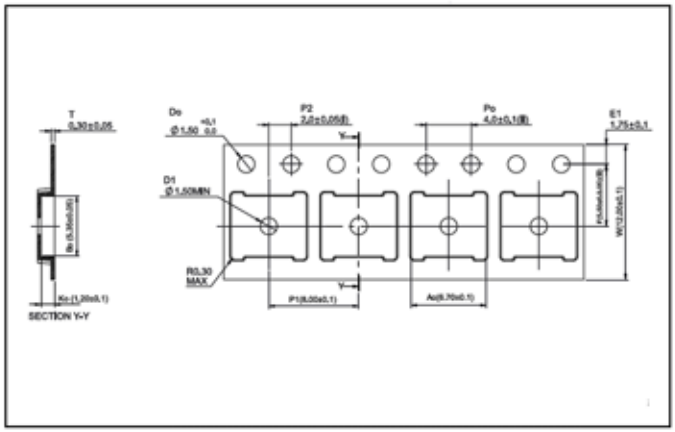
Packing Information



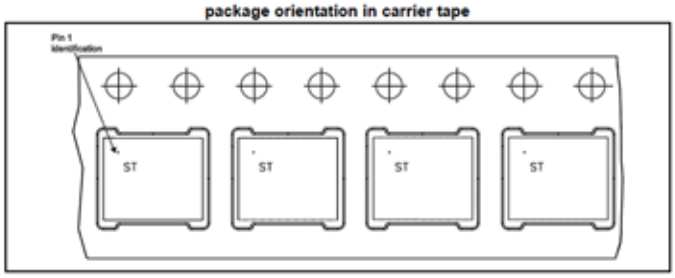
package orientation in carrier tape



Packing Information



package orientation in carrier tape

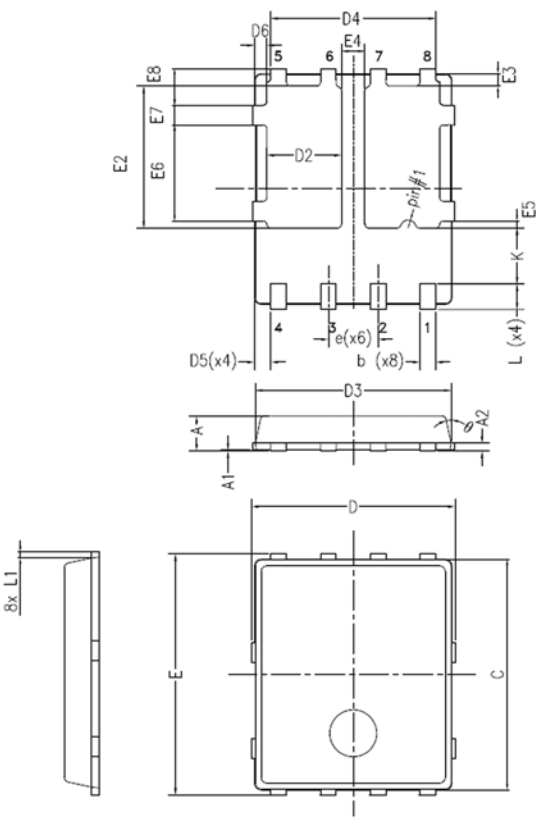


Remark: Comparison done with real Package, current and Wettable Flanks
It may be different from previous drawing, present in some datasheet

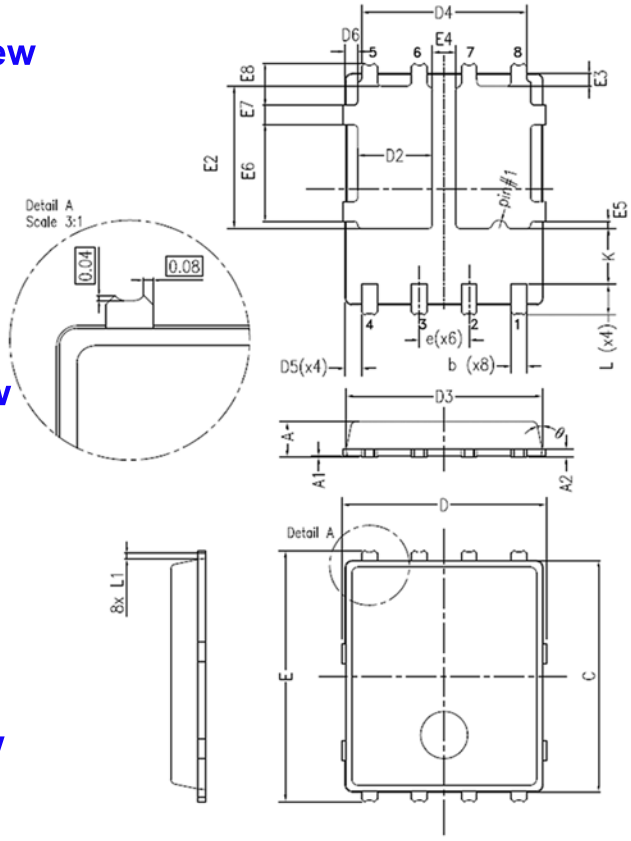
PowerFLAT™ 5x6 double island

Type R (Ribbon)

Current



Wettable Flanks



DIMENSIONS				
REF. DIM	DATA BOOK (mm)			NOTES
	NOM	MIN	MAX	
A		0.80	1.00	
A1		0.02	0.05	
A2	0.25			
b		0.30	0.50	
C	6.00	5.80	6.20	
D	5.20	5.00	5.40	
D2		1.68	1.88	
D3	5.00	4.80	5.20	
D4	4.20	4.05	4.35	
D5	0.40	0.25	0.55	
D6	0.30	0.15	0.45	
e	1.27			
E	6.15	5.95	6.35	
E2		3.50	3.70	
E3	0.325	0.20	0.45	
E4		0.55	0.75	
E5		0.08	0.28	
E6		2.35	2.55	
E7		0.40	0.60	
E8	0.90	0.75	1.05	
K		1.275	1.575	
L		0.60	0.80	
L1	0.15	0.05	0.25	
θ		0°	12°	

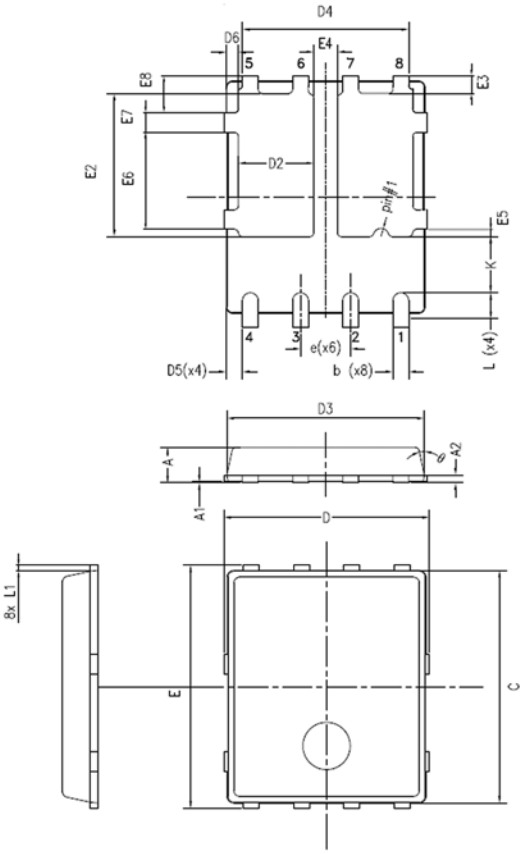
DIMENSIONS				
REF. DIM	DATA BOOK (mm)			NOTES
	NOM	MIN	MAX	
A		0.80	1.00	
A1		0.02	0.05	
A2	0.25			
b		0.30	0.50	
C	6.00	5.80	6.20	
D	5.20	5.00	5.40	
D2		1.68	1.88	
D3	5.00	4.80	5.20	
D4	4.20	4.05	4.35	
D5	0.40	0.25	0.55	
D6	0.30	0.15	0.45	
e	1.27			
E	6.40	6.20	6.60	
E2		3.50	3.70	
E3	0.325	0.20	0.45	
E4		0.55	0.75	
E5		0.08	0.28	
E6		2.35	2.55	
E7		0.40	0.60	
E8	1.00	0.85	1.15	
K		1.275	1.575	
L		0.70	0.90	
L1	0.275			
θ		0°	12°	

Remark: Comparison done with real Package, current and Wettable Flanks.
It may be different from previous drawing, present in some datasheet.

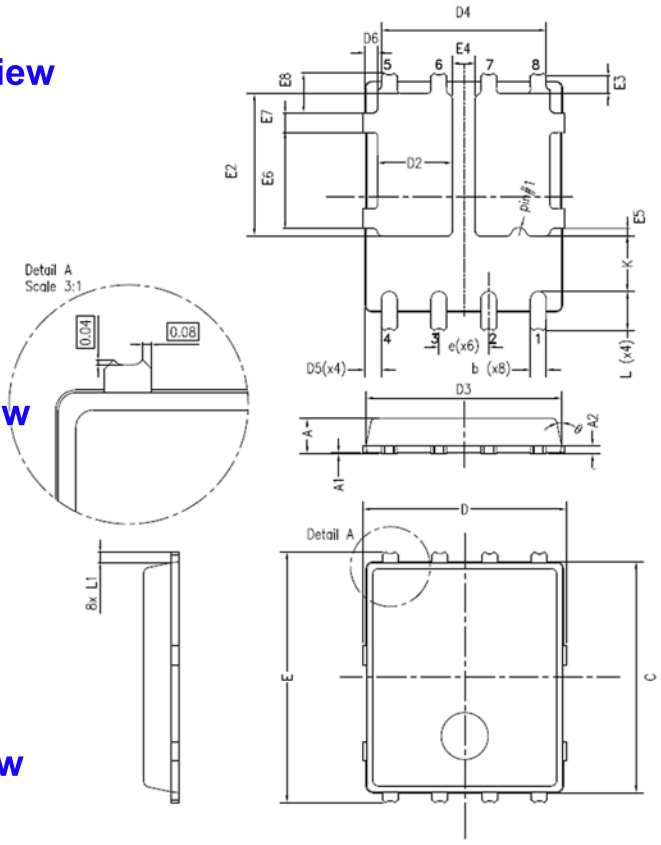
PowerFLAT™ 5x6 double island

Type C (Clip)

Current



Wettable Flanks



DIMENSIONS				
REF. DIM	DATA BOOK (mm)			NOTES
	NOM	MIN	MAX	
A		0.80	1.00	
A1		0.02	0.05	
A2	0.25			
b		0.30	0.50	
C	6.00	5.80	6.20	
D	5.20	5.00	5.40	
D2		1.68	1.88	
D3	5.00	4.80	5.20	
D4	4.20	4.05	4.35	
D5	0.40	0.25	0.55	
D6	0.30	0.15	0.45	
e	1.27			
E	6.15	5.95	6.35	
E2		3.50	3.70	
E3	0.325	0.20	0.45	
E4		0.55	0.75	
E5		0.08	0.28	
E6		2.35	2.55	
E7		0.40	0.60	
E8	0.90	0.75	1.05	
K		1.05	1.35	
L		0.725	1.025	
L1	0.15	0.05	0.25	
θ		0°	12°	

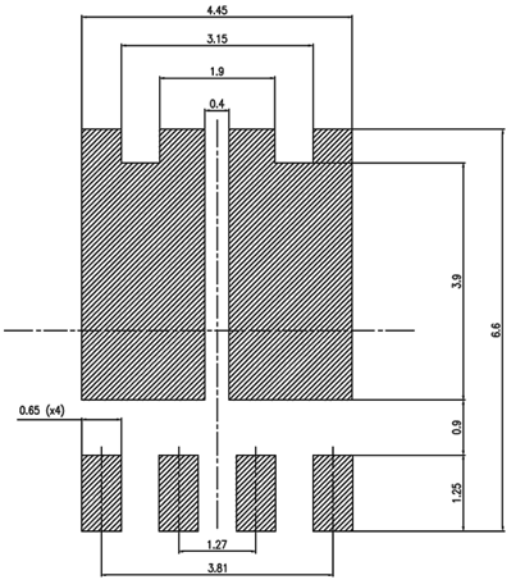
DIMENSIONS				
REF. DIM	DATA BOOK (mm)			NOTES
	NOM	MIN	MAX	
A		0.80	1.00	
A1		0.02	0.05	
A2	0.25			
b		0.30	0.50	
C	6.00	5.80	6.20	
D	5.20	5.00	5.40	
D2		1.68	1.88	
D3	5.00	4.80	5.20	
D4	4.20	4.05	4.35	
D5	0.40	0.25	0.55	
D6	0.30	0.15	0.45	
e	1.27			
E	6.40	6.20	6.60	
E2		3.50	3.70	
E3	0.325	0.20	0.45	
E4		0.55	0.75	
E5		0.08	0.28	
E6		2.35	2.55	
E7		0.40	0.60	
E8	1.00	0.85	1.15	
K		1.05	1.35	
L		0.90	1.10	
L1	0.275	0.175	0.375	
θ		0°	12°	

Remark: Comparison done with real Package, current and Wettable Flanks.
It may be different from previous drawing, present in some datasheet.

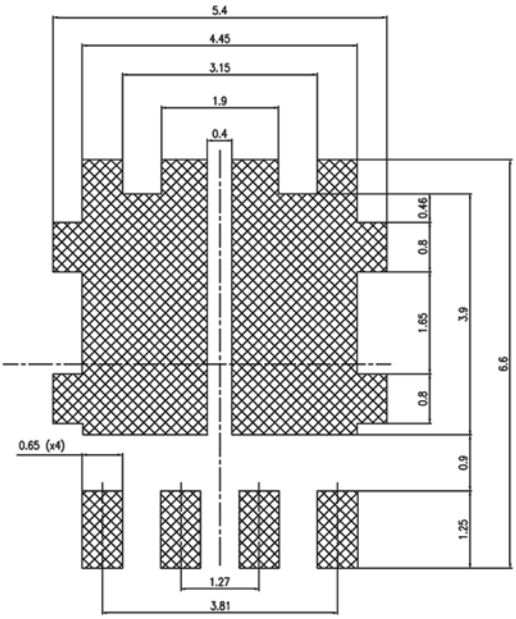
PowerFLAT™ 5x6 double island

Footprint

Current

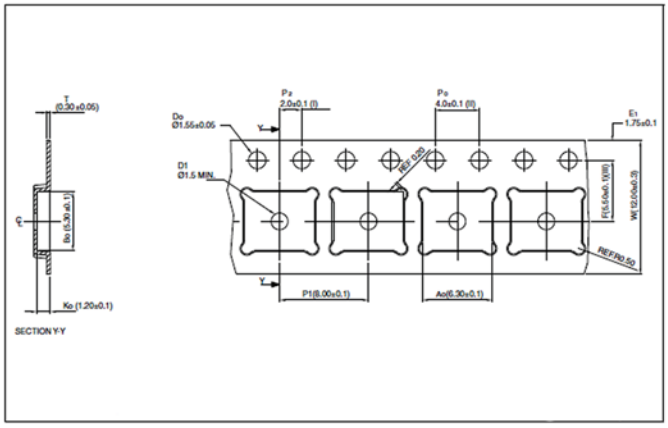


Wettable Flanks

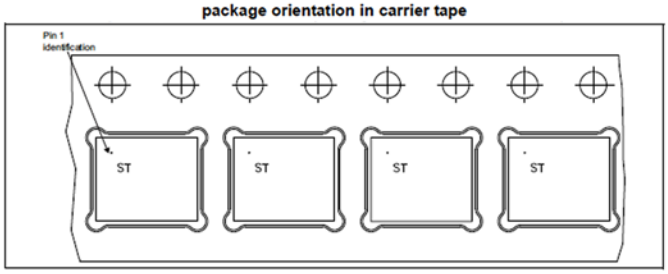


Carrier Tape

Packing Information



package orientation in carrier tape



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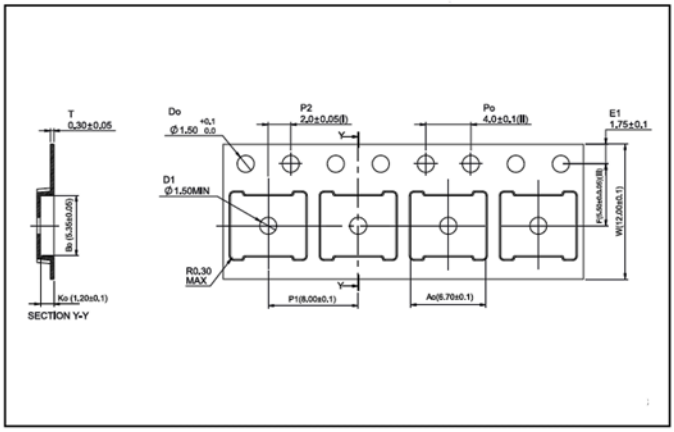
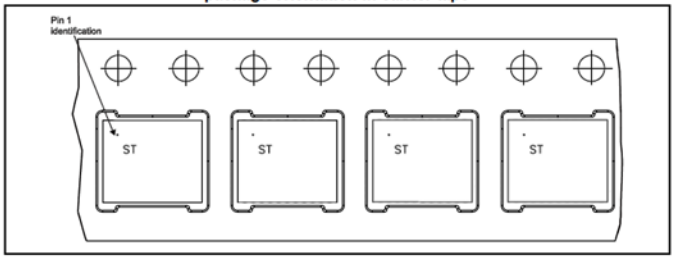


package orientation in carrier tape



Remark: Comparison done with real Package, current and Wettable Flanks
It may be different from previous drawing, present in some datasheet

Dear Customer,

Please be informed that, in order to facilitate side wetting to meet automotive requirement for visual inspection, PowerFLAT™ 5x6 of Power MOSFET Transistors for Automotive application, manufactured in Shenzhen (China) will be produced with wettable flanks package.

The involved product series and affected packages are listed in the table below:

Product Family Description	Package	Commercial Product / Series
Power MOSFET Transistors	PowerFLAT™ 5x6	STLxxxxxxx

Any other Product related to the above series, manufactured in PowerFLAT™ 5x6 Package, even if not expressly included or partially mentioned in the attached table, is affected by this change.

Qualification program and results availability:

The reliability test report is provided in attachment to this document.

Samples availability:

Samples of the test vehicle devices will be available on request starting from week 48-2015.
Any other sample demand will be processed and scheduled by Power Transistor Division upon request.

Product Family Description	Part Number - Test Vehicle
Power MOSFET Transistors	STL120N4F6AG * STL120N4LF6AG * STL15DN4F5 STL40DN3LLH5 STL66N3LLH5 STL8DN6LF3 STL8N10LF3

* These products are Test Vehicles used for qualification only, they are not involved by the change because were born wettable flanks.

Change implementation schedule:

The production start and first shipments will be implemented according to our work in progress and materials availability:

Product Family Description	Estimate 1st Shipments
Power MOSFET Transistors	From Week 21-2016

Marking and traceability:

Unless otherwise stated by customer specific requirement, traceability of PowerFLAT™ 5x6 Package wettable flanks, manufactured in Shenzhen (China), will be identified by date-code.

Sincerely Yours.

FINAL
Reliability Report
PowerFLAT™ 5x6 Automotive wettable flanks – Shenzhen (China).

General Information	
Product Lines:	4L0C – 4L63 D.I. - 5H3A D.I. – 5H3C - 5D4P D.I. - 6L4F – 6D4F
Product Families:	Power MOSFET
P/Ns:	STL8N10LF3 (4L0C) STL8DN6LF3 (4L63 D.I.) STL66N3LLH5 (5H3C) STL40DN3LLH5 (5H3A D.I.) STL15DN4F5 (5D4P D.I.) STL120N4LF6AG (6L4F) STL120N4F6AG (6D4F)
Product Group:	IPG
Product division:	Power Transistor Division
Package:	PowerFLAT™ 5x6 8L WF
Silicon Process techn.:	STripFET™ LV Power MOSFET

Locations	
Wafer Diffusion Plant:	*Ang Mo Kio (Singapore)* : 4L0C – 4L63 Catania: 5H3C – 5H3A – 5D4P – 6L4F – 6D4F
EWS Plant:	*Ang Mo Kio (Singapore)* *Catania (Italy)*
Assembly and testing plant:	*ST Shenzhen (China)*
Reliability Lab:	*IPG-PTD Catania Reliability Lab.*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	February 2015	13	A.Settinieri	C. Cappello	First issue

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q101 Rev.D1	Stress test qualification for automotive grade discrete semiconductors
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size
HF	Halogen Free

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Reliability evaluation for AUTOMOTIVE LV Power MOSFET transistors assembled in PowerFLAT™ 5x6 wettable flanks package of ST Shenzhen plant.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

N-channel LV Power MOSFET

4.2 Construction note

D.U.T.: STL8N10LF3 LINE: 4L0C PACKAGE: PowerFLAT™ 5x6

Wafer/Die fab. Information	
Wafer fab manufacturing location	Ang Mo Kio (Singapore)
Technology	STripFET™ III Power MOSFET
Die finishing back side	Ti/Ni/Ag
Die size	3220 x 1550 µm^2
Metal	AlSiCu
Passivation type	TEOS + Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Ang Mo Kio (Singapore)
Test program	WPIS

Assembly information	
Assembly site	ST Shenzhen (China)
Package description	PowerFLAT™ 5x6 WF
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	Al Gate – RIBBON Source
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	ST Shenzhen (China)
Tester	IP Tester

D.U.T.: STL8DN6LF3 LINE: 4L63 D.I. PACKAGE: PowerFLAT™ 5x6

Wafer/Die fab. Information	
Wafer fab manufacturing location	Ang Mo Kio (Singapore)
Technology	STripFET™ III Power MOSFET
Die finishing back side	Ti/Ni/Au
Die size	2490 x 1550 µm^2
Metal	AlSiCu
Passivation type	TEOS + Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Ang Mo Kio (Singapore)
Test program	WPIS

Assembly information	
Assembly site	ST Shenzhen (China)
Package description	PowerFLAT™ 5x6 WF
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	Al Gate – RIBBON Source
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	ST Shenzhen (China)
Tester	IP Tester

D.U.T.: STL66N3LLH5 LINE: 5H3C PACKAGE: PowerFLAT™ 5x6

Wafer/Die fab. Information	
Wafer fab manufacturing location	Catania (Italy)
Technology	STripFET™ V Power MOSFET
Die finishing back side	Ti/NiV/Ag
Die size	2500 x 1820 µm^2
Metal	AlCu(Catania)+TiNiAu(Tours)
Passivation type	USG+TEOS

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Catania (Italy)
Test program	WPIS

Assembly information	
Assembly site	ST Shenzhen (China)
Package description	PowerFLAT™ 5x6 WF
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	Au Gate – CLIP Source
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	ST Shenzhen (China)
Tester	IP Tester

D.U.T.: STL40DN3LLH5 LINE: 5H3A D.I PACKAGE: PowerFLAT™ 5x6

Wafer/Die fab. Information	
Wafer fab manufacturing location	Catania (Italy)
Technology	STripFET™ V Power MOSFET
Die finishing back side	Ti/NiV/Ag
Die size	1640 x 1060 µm^2
Metal	AlCu
Passivation type	TEOS + Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Catania (Italy)
Test program	WPIS

Assembly information	
Assembly site	ST Shenzhen (China)
Package description	PowerFLAT™ 5x6 WF
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	Al Gate – RIBBON Source
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	ST Shenzhen (China)
Tester	IP Tester

D.U.T.: STL15DN4F5 LINE: 5D4P D.I PACKAGE: PowerFLAT™ 5x6

Wafer/Die fab. Information	
Wafer fab manufacturing location	Catania (Italy)
Technology	STripFET™ V Power MOSFET
Die finishing back side	Ti/NiV/Ag
Die size	2500 x 1690 µm^2
Metal	AlCu(Catania)+TiNiAu(Tours)
Passivation type	USG+TEOS

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Catania (Italy)
Test program	WPIS

Assembly information	
Assembly site	ST Shenzhen (China)
Package description	PowerFLAT™ 5x6 WF
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	Au Gate – CLIP Source
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	ST Shenzhen (China)
Tester	IP Tester

D.U.T.: STL120N4LF6AG LINE: 6L4F PACKAGE: PowerFLAT™ 5x6

Wafer/Die fab. Information	
Wafer fab manufacturing location	Catania (Italy)
Technology	STripFET™ VI Power MOSFET
Die finishing back side	Ti/NiV/Au
Die size	3860 x 2640 μm^2
Metal	AlCu
Passivation type	TEOS + Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Catania (Italy)
Test program	WPIS

Assembly information	
Assembly site	ST Shenzhen (China)
Package description	PowerFLAT™ 5x6 WF
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	Al Gate – RIBBON Source
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	ST Shenzhen (China)
Tester	IP Tester

D.U.T.: STL120N4F6AG LINE: 6D4F PACKAGE: PowerFLAT™ 5x6

Wafer/Die fab. Information	
Wafer fab manufacturing location	Catania (Italy)
Technology	STripFET™ V I Power MOSFET
Die finishing back side	Ti/NiV/Au
Die size	3860 x 2640 μm^2
Metal	AlCu
Passivation type	TEOS + Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Catania (Italy)
Test program	WPIS

Assembly information	
Assembly site	ST Shenzhen (China)
Package description	PowerFLAT™ 5x6 WF
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	Al Gate – RIBBON Source
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	ST Shenzhen (China)
Tester	IP Tester

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	line	Tech.	package	Comments
1	4L0C	EDD3	PowerFLAT™ 5x6 WF	Power MOSFET LV AUTOMOTIVE
2	4L63 D.I.			
3	4L63 D.I.			
4	5H3C	EHD5		
5	5H3A D.I.			
6	5D4P D.I.			
7	6L4F	LVT1		
8	6D4F			

5.2 Reliability test plan summary

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS							
						LOT1	LOT2 D.I	LOT3 D.I	LOT4	LOT5 D.I	LOT6 D.I	LOT7	LOT8
Die Oriented Tests													
TEST			All qualification parts tested per the requirements of the appropriate device spec.			154	770	308	231	924	924	462	231
External Visual			All devices submitted for testing			154	770	308	231	924	924	462	231
Parametric Verification			all parameters according to user specification from -55°C to 175°C			0/25	0/25	0/25	0/25	0/25	0/25	0/25	0/25
HTRB	**N**	**JESD22 A-108**	**TA = 175°C, BIAS=48V (LOT1-2-3) * BIAS=30V (LOT3-4) BIAS=40V (LOT5-6)**	693	168 H	-	0/154	-	0/77	0/154	0/154	0/77	0/77
					500 H	-	0/154	-	0/77	0/154	0/154	0/77	0/77
					1000 H	-	0/154	-	0/77	0/154	0/154	0/77	0/77
HTFB	**N**	**JESD22 A-108**	**TA = 175°C, BIAS = 20V (LOT1-2-3-6-7) BIAS = 22V (LOT3-4-5)**	693	168 H	-	0/154	-	0/77	0/154	0/154	0/77	0/77
					500 H	-	0/154	-	0/77	0/154	0/154	0/77	0/77
					1000 H	-	0/154	-	0/77	0/154	0/154	0/77	0/77
PC		**JESD22 A-113**	**Drying 24 H @ 125°C Store 168 H @ TA=85°C Rh=85% Over Reflow @ Tpeak=260°C 3 times**	All devices to be subjected to H3TRB, TC, AC, IOL		pass	pass	pass	pass	pass	pass	pass	pass
AC	**Y**	**JESD22 A-102**	**Pa=2Atm / TA=121°C**	924	96 H	0/77	0/154	0/154	0/77	0/154	0/154	0/77	0/77
TC	**Y**	**JESD22 A-104**	**TA = -55°C to 150°C**	770	100 cy	0/77	0/154	0/154	-	0/154	0/154	0/77	-
					200 cy	0/77	0/154	0/154	-	0/154	0/154	0/77	-
					500 cy	0/77	0/154	0/154	-	0/154	0/154	0/77	-
					1 Kcy	0/77	0/154	0/154	-	0/154	0/154	0/77	-
TCHT	**Y**	**JESD22 A-104 Appendix 6**	**125°C TEST after TC**	385		-	-	-	-	0/154	0/154	0/77	-
			decap and wire pull for parts with internal bond wire sizes 5 mil diameter and less	15		-	-	-	-	0/5	0/5	0/5	-

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS							
						LOT1	LOT2	LOT3	LOT4	LOT5	LOT6	LOT7	LOT8
TCDT	Y		100% C-SAM inspection after TC	385						0/154	0/154	0/77	
H3TRB	Y	JESD22 A-101	TA=85°C , RH=85% , BIAS= 50V	539	168 H	-	0/154	-	-	0/154	0/154	0/77	-
					500 H	-	0/154	-	-	0/154	0/154	0/77	-
					1000 H	-	0/154	-	-	0/154	0/154	0/77	-
IOL / TF	Y	MIL-STD-750 Method 1037	ΔTC=105°C Ton / Toff = 2 min	385	15Kcy	-	-	-	-	0/154	0/154	0/77	-
D.P.A.		AEC-Q101-004 Section 4	Devices after H3TRB - TC	12		-	-	-	-	0/4	0/4	0/4	-
Physical Dimension		JESD22 B-100		90		0/30	-	-	-	0/30		0/30	-
Solderability		J-STD-002		30		-	-	-	-	0/10	0/10	0/10	-
Die Shear		AEC-Q101-003		30	10 bonds from min of 5 devices	0/10	-	-	-	0/10	-	0/10	-
Thermal Resistance		JESD24-3, 24-4, 24-6 as appropriate		30	10 pre & post change	0/10	-	-	-	0/10	-	0/10	-
Dielectric Integrity		AEC-Q101-004		15		0/5	-	-	-	0/5	-	0/5	-

*. Reliability test performed as per AEC-Q101 Rev.C guidelines – Assessment performed before Rev.D1 introduction.

6 ANNEXES 6.0

6.1Tests Description

Test name	Description	Purpose
Die Oriented Tests		
HTRB High Temperature Reverse Bias **HTGB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: • low power dissipation; • max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
Package Oriented Tests		
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
TF / IOL Thermal Fatigue / Intermittent Operating Life	The device is submitted to cycled temperature excursions generated by power cycles (ON/OFF) at T ambient.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
H3TRB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	To verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.